A High Gain Single Input Multiple Output Boost Converter

Anuja Ann Mathews¹, Prof. Acy M Kottali², Prof. George John P³

¹PG Scholar, ²,³Professor
¹,²,³Department of Electrical, Electronics Engineering, Mar Athanasius College of Engineering, Kothamangalam, Kerala, India

Abstract: This converter is a newly designed single input multiple output DC-DC converters with coupled inductor. This converter uses only one power switch. This topology has two boost converters. One is a high gain converter and other is a normal boost converter. The techniques of voltage clamping is used to reduce the switching loss and conduction loss. For the high gain converter the energy stored in the leakage inductance of coupled inductor is efficiently recycled to the output. As a result high voltage conversion ratio is obtained. By using this converter, high efficiency power conversion, high step up ratio, and various output voltages with different levels can be obtained. The simulation is carried out in MATLAB/SIMULINK.

Keywords: Boost converter, coupled inductor, high gain converter, voltage clamp circuit, voltage doubler cell, voltage stress.

I. INTRODUCTION

There are various single-input single-output DC-DC converters with different voltage gains are combined to satisfy the requirement of various voltage levels, so that its system control is more complicated and the corresponding cost is more expensive. The motivation of this study is to design a single-input multiple-output (SIMO) converter for increasing the conversion efficiency and voltage gain, reducing the control complexity, and saving the manufacturing cost.

This high gain converter can boost the voltage of a low voltage input power source to a controllable high-voltage DC and middle-voltage output terminals. The high voltage DC can be taken as the main power for a high-voltage DC load or the front terminal of a DC-AC inverter. Moreover, middle voltage output terminals can supply powers for individual middle-voltage DC loads or for charging auxiliary power sources (e.g., battery modules) [6]. In this study, a coupled-inductor based DC-DC converter scheme utilizes only one power switch with the properties of voltage clamping and the corresponding device specifications are adequately designed.

II. HIGH GAIN SINGLE INPUT MULTIPLE OUTPUT BOOST CONVERTER

This converter has two boost converters. One is a high gain converter and the other is a middle voltage converter. This converter makes use of a single power switch Q, an input inductor L₁ and a coupled inductor, diodes D₁, D₂, D₃ and D₀, a storage energy capacitor C₁ and a output capacitor Cₐ₁ and Cₐ₂, a clamp circuit including diode D₃ and capacitor C₂, an extended voltage doubler cell comprising regeneration diode Dₚ and capacitor Cₚ, and the secondary side of the coupled inductor. The dual-winding coupled inductor is modeled as an ideal transformer with a turn ratio N (n₂/n₁), a parallel magnetizing inductance Lₚ and primary and secondary leakage inductance Lₚ₁ and Lₚ₂ respectively. Figure 2 shows the detailed circuit diagram of the high gain converter.

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Figure 1: Circuit diagram of high gain single input multiple output boost converter

Figure 2: Circuit diagram of high gain converter in detail

For analysis of the converter, the assumptions are input inductance $L_1$ is very large enough so that $i_{L1}$ is continuous.

A. DIFFERENT MODES OF OPERATION:

MODE 1:

During this time interval $[t_0, t_1]$, the switch Q is conducting at $t = t_0$. Diodes $D_1, D_3$ and $D_0$ are reverse-biased by $V_{c1}, V_{c1} + V_{c2}$ and $V_0 - V_{c1} - V_{c2}$ respectively. Diode $D_4$ is also in off condition. Only Diodes $D_2$ and $D_r$ are turned ON. Figure 3 shows the current flow path. The dc source $V_{in}$ energy is transferred to the inductor $L_1$ through $D_2$ and Q. Therefore, current $i_{L1}$ is increasing linearly. The primary voltage of the coupled inductor including magnetizing inductor $L_m$ and...
leakage $L_{k1}$ is $V_{c1}$ and the capacitor $C_1$ is discharging its energy to the magnetizing inductor $L_m$ and primary leakage inductor $L_{k1}$ through $Q$.

Then currents $i_{D2}$, $i_{Lm}$, and $i_{k1}$ are increasing. Meanwhile, the energy stored in $C_2$ and $C_1$ is released to $C_3$ through $D_r$. The loads $R_1$ and $R_2$ are supplied by the output capacitors $C_{01}$ and $C_{02}$ respectively. This stage ends at $t = t_1$.

MODE 2:

In this interval, $Q$ is turned off at $t = t_1$, the current through $Q$ is forced to flow through $D_3$. At the same time, the energy stored in inductor $L_1$ flows through diode $D_1$ to charge capacitor $C_1$ instantaneously and also through diode $D_4$. The inductor current $i_{L1}$ declines linearly. Thus, the diode $D_2$ is reverse biased by $V_{c2}$. A part of inductor current $i_{L1}$ also flows through $D_4$. The diode $D_0$ is still reverse biased by $V_{D0} - V_{c1} - V_{c2}$. The energy stored in inductor $L_{k1}$ flows through diode $D_3$ to charge capacitor $C_2$. Therefore, the energy stored in $L_{k1}$ is recycled to $C_2$. The $L_{k2}$ keeps the same current direction for charging capacitor $C_3$ through diode $D_3$ and regeneration-diode $D_r$. The load energy is supplied by the output capacitors $C_{01}$. Figure 4 shows the current flow path of this mode.
MODE 3:
During this transition interval, switch Q remains OFF. \( V_{C2} \) is reflected to the secondary side of coupled inductor thus, regeneration-diode Dr is blocked by \( V_{C3} + NV_{C2} \). Meanwhile, the diode \( D_0 \) starts to conduct. Figure 5 shows the current flow path of this mode. The inductance \( L_1 \) is still releasing its energy to the capacitor \( C_1 \). Thus, the current \( i_{L1} \) still declines linearly. The energy stored in \( L_{k1} \) and \( L_m \) is released to \( C_2 \). Also a part of energy stored in \( L_1 \) and \( L_{k1} \) is released to \( C_02 \) and \( R_2 \) through \( D_4 \). Moreover, the energy stored in \( L_m \) is released to the output via \( n_2 \) and \( C_3 \). The leakage inductor energy can thus be recycled, and the voltage stress of the main switch is clamped to the summation of \( V_{C1} \) and \( V_{C2} \).

MODE 4:
During this time interval, the switch Q, diodes \( D_2 \) and Dr is still turned OFF. Since \( i_{C2} \) reaches zero at \( t = t_3 \), the entire current of \( i_{L1} \) flows through \( D_3 \) is blocked. The current flow path of this mode is shown in figure 6. The energy stored in an inductor \( L_1 \) flows through diode \( D_1 \) to charge capacitor \( C_1 \) continually, so the current \( i_{L1} \) is decreasing linearly. Also a part of energy stored in \( L_1 \) and \( L_{k1} \) is released to \( C_02 \) and \( R_2 \) through \( D_4 \). The dc source \( V_{in} , L_1 , L_m , L_{k1}, \) the winding \( n_2, L_{k2} \) and \( V_{c3} \) are series connected to discharge their energy to capacitor \( C_{01} \) and load \( R_1 \). This stage ends when the switch Q is turned ON at \( t = t_4 \).
MODE 5:
The main switch Q is turned ON at t4. During this transition interval, diodes D1, D3, and D4 are reverse-biased $V_{c1}$, $V_{c1} + V_{c2}$ and $V_{c2} - V_{c1} - V_{c2}$ respectively. D4 is also in off condition. The current flow path is shown in Figure 7. The inductance $L_1$ is charged by input voltage $V_{in}$ and the current $i_{L1}$ increases almost in a linear way. The blocking voltages $V_{c1}$ is applied on magnetizing inductor $L_m$ and primary-side leakage $L_{k1}$, so the current $i_{Lk1}$ of the coupled inductor is increased rapidly. Meanwhile, the magnetizing inductor $L_m$ keeps on transferring its energy through the secondary winding to the output capacitor $C_{01}$ and load $R_1$. At the same time, the energy stored in $C_3$ is discharged to the output 1. $R_2$ is fed by $C_{02}$.

Figure 8. Current flow in mode 5

III. SIMULATION RESULTS

Table 1. Simulation Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input inductor L1</td>
<td>16 µH</td>
</tr>
<tr>
<td>C1, C0</td>
<td>100 µF</td>
</tr>
<tr>
<td>C2, C3</td>
<td>47 µF</td>
</tr>
<tr>
<td>Coupled inductor</td>
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<tr>
<td>Turns ratio</td>
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<td>Primary winding inductance</td>
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<tr>
<td>Secondary winding inductance</td>
<td>186 µH</td>
</tr>
<tr>
<td>$L_m$</td>
<td>100 µH</td>
</tr>
<tr>
<td>Switch</td>
<td>MOSFET</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>40 kHz</td>
</tr>
<tr>
<td>Duty ratio</td>
<td>0.4</td>
</tr>
</tbody>
</table>
Figure 9. Simulink model of high gain single input multiple output boost converter

Figure 10. Gate pulse

Figure 11. Converter output voltages
By giving an input of 5 V, two output voltages are obtained. One is the high gain output 54 V and the other is the middle voltage output 14 V. Voltage stress across the switch is 12 V.

IV. CONCLUSIONS

A high gain single input multiple output DC-DC converter is introduced. The simulation result shows that single input power source is converted to two output terminals. This topology adopts only one power switch to achieve the objective of multiple output. The voltage stress across the switch is only 22% of the high gain output. The technique of voltage clamping is used to reduce the switching and conduction losses. The energy stored in the leakage inductance of coupled inductor efficiently recycled to one of the output. This topology provides the designers with an alternative choice for boosting a low-voltage power source to multiple outputs with different voltage levels efficiently.

REFERENCES


